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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/039,789	01/02/2002	David K. Poulsen	INTL-0663-US (P12629)	9218

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EXAMINER	
YIGDALL, MICHAEL J	

ART UNIT	PAPER NUMBER
2122	

DATE MAILED: 12/14/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/039,789	POULSEN ET AL.	
	Examiner	Art Unit	
	Michael J. Yigdall	2122	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 January 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 January 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *5/8/02*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-20 are pending and have been examined. The priority date considered for the application is January 2, 2002.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Pat. No. 5,812,852 to Poulsen et al. (hereinafter "Poulsen") in view of U.S. Pat. No. 5,937,194 to Sundaresan (hereinafter "Sundaresan").

With respect to claim 1, Poulsen discloses a method comprising:

(a) receiving a first program unit in a parallel computing environment (see, for example, column 8, lines 29-30, which shows receiving a parallel computer program unit).

Although Poulsen discloses that the program includes parallel regions and global storage objects (see, for example, column 8, lines 29-30), Poulsen does not expressly disclose the limitation wherein the first program unit includes a reduction operation associated with a set of variables.

However, Sundaresan discloses a reduction operation associated with a set of values or variables, wherein the reduction operation performs an algebraic operation on the values or

variables and is partitioned among a plurality of threads (see, for example, column 7, lines 13-16, and column 1, lines 59-63). The reduction operation in Sundaresan is implemented with reusable reduction objects so as to improve the expressibility and maintenance of parallel code (see, for example, column 5, lines 7-14, 21-23 and 30-33).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the system of Poulsen to include a reduction operation, such as with the reusable reduction objects taught by Sundaresan, for the purpose of improving the expressibility and maintenance of the parallel computer program.

Therefore, Poulsen in view of Sundaresan discloses receiving a first program unit in a parallel computing environment, the first program unit including a reduction operation associated with a set of variables.

Poulsen in view of Sundaresan further discloses:

(b) translating the first program unit into a second program unit, the second program unit to associate the reduction operation with a set of one or more instructions operative to partition the reduction operation between a plurality of threads including at least two threads (see, for example, Poulsen, column 8, lines 32-35, which shows translating the program, and Sundaresan, column 7, lines 13-16, which shows that the reduction operation is partitioned among a plurality of threads, as presented above); and

(c) translating the first program unit into a third program unit, the third program unit to associate the reduction operation with a set of one or more instructions operative to perform an algebraic operation on the variables (see, for example, Poulsen, column 8, lines 32-35, which shows translating the program, and Sundaresan, column 7, lines 13-16, and column 1, lines 59-

63, which shows that the reduction operation performs an algebraic operation on the values or variables, as presented above).

With respect to claim 2, Poulsen in view of Sundaresan further discloses encapsulating the reduction operation with the instructions associated with the third program unit (see, for example, Poulsen, column 8, lines 46-47 and 59-61, which shows encapsulating objects when translating the program).

With respect to claim 3, Poulsen in view of Sundaresan further discloses reducing the variables logarithmically (see, for example, Sundaresan, column 7, lines 16-18, which shows that the reduction operation reduces the values or variables logarithmically).

With respect to claim 4, Poulsen in view of Sundaresan further discloses translating the first program unit into the second program unit utilizing, in part, a source-code to source-code translator (see, for example, Poulsen, column 8, lines 35-37, which shows translating the program with a source-to-source translator).

With respect to claim 5, Poulsen in view of Sundaresan further discloses translating the first program unit into the third program unit utilizing, in part, a source-code to source-code translator (see, for example, Poulsen, column 8, lines 35-37, which shows translating the program with a source-to-source translator).

With respect to claim 6, Poulsen in view Sundaresan further discloses associating the plurality of threads each with a unique portion of the set of variables (see, for example,

Sundaresan, column 7, lines 20-21, which shows that the reduction operation associates individual values or variables to each of the threads).

With respect to claim 7, Poulsen in view of Sundaresan further discloses combining, in part, the variables associated with the plurality of threads in a pair-wise reduction operation (see, for example, Sundaresan, column 11, line 48 to column 12, line 7, which shows a sample reduction operation that combines the values or variables associated with the plurality of threads in a pair-wise reduction operation, wherein a given thread has a fan-in of two threads, which is to say a pair of threads).

With respect to claim 8, Poulsen discloses an apparatus comprising:

(a) a memory including a shared memory location (see, for example, column 8, lines 37-39, which shows a memory, and column 7, lines 7-10, which shows a global storage object in a shared memory location);

(b) a translation unit coupled with the memory (see, for example, column 8, lines 32-35, which shows a translation means).

Although Poulsen discloses a parallel computer program unit (see, for example, column 8, lines 29-30) and further discloses translating the program (see, for example, column 8, lines 32-35), Poulsen does not expressly disclose the limitation wherein the translation unit is to translate a first program unit including a reduction operation associated with a set of at least two variables into a second program unit, the second program unit to associate the reduction operation with one or more instructions operative to partition the reduction operation between a plurality of threads including at least two threads.

However, Sundaresan discloses a reduction operation associated with a set of values or variables, wherein the reduction operation performs an algebraic operation on the values or variables and is partitioned among a plurality of threads (see, for example, column 7, lines 13-16, and column 1, lines 59-63). The reduction operation in Sundaresan is implemented with reusable reduction objects so as to improve the expressibility and maintenance of parallel code (see, for example, column 5, lines 7-14, 21-23 and 30-33).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the system of Poulsen to include a reduction operation, such as with the reusable reduction objects taught by Sundaresan, for the purpose of improving the expressibility and maintenance of the parallel computer program.

Therefore, Poulsen in view of Sundaresan discloses a translation unit coupled with the memory, the translation unit to translate a first program unit including a reduction operation associated with a set of at least two variables into a second program unit, the second program unit to associate the reduction operation with one or more instructions operative to partition the reduction operation between a plurality of threads including at least two threads.

Poulsen in view of Sundaresan further discloses:

(c) a compiler unit coupled with the translation unit and the shared-memory, the compiler unit to compile the second program unit (see, for example, Poulsen, column 8, lines 42-45, which shows an executable program, which is to say a compiled program, and column 13, lines 11-13, which shows that the translation may be integrated with a compiler); and

(d) a linker unit coupled with the compiler unit and the shared-memory, the linker unit to link the compiled second program with a library (see, for example, Poulsen, column 8, lines 39-42, which shows a linker for linking the program with a library).

With respect to claim 9, Poulsen in view of Sundaresan further discloses the limitation wherein the second program unit associates a set of one or more instructions with the reduction operative to encapsulate the reduction operation (see, for example, Poulsen, column 8, lines 46-47 and 59-61, which shows encapsulating objects when translating the program).

With respect to claim 10, Poulsen in view of Sundaresan further discloses the limitation wherein the variables in the set of variables are each uniquely associated with the plurality of threads and the library includes instructions operative to combine, in part, the variables associated with the plurality of threads (see, for example, Poulsen, column 10, lines 9-11 and 15-19, which shows that instructions in the library are called for each parallel region in the program, and Sundaresan, column 7, lines 20-21, which shows that the reduction operation associates individual values or variables to each of the threads).

With respect to claim 11, Poulsen in view of Sundaresan further discloses the limitation wherein the library includes instructions operative to combine, in part, the variables in a pair-wise reduction (see, for example, Sundaresan, column 11, line 48 to column 12, line 7, which shows a sample reduction operation that combines the values or variables associated with the plurality of threads in a pair-wise reduction operation, wherein a given thread has a fan-in of two threads, which is to say a pair of threads).

With respect to claim 12, Poulsen in view of Sundaresan further discloses a set of one or more processors to host the plurality of threads, the plurality of threads to execute instructions associated with the second program unit (see, for example, Poulsen, column 6, lines 46-50, which shows one or more processors for executing the plurality of threads).

With respect to claim 13, Poulsen in view of Sundaresan further discloses the limitation wherein the second program includes a callback routine and the callback routine is associated with instructions operative to perform an algebraic operation on at least two variables in the set of variables (see, for example, Poulsen, column 9, line 63 to column 10, line 9, which shows callback routines for the parallel regions in the program, and Sundaresan, column 7, lines 13-16, and column 1, lines 59-63, which shows that the reduction operation performs an algebraic operation on the values or variables).

With respect to claim 14, Poulsen in view of Sundaresan further discloses the apparatus of claim 13 wherein the library is operative to call the callback routine to perform, in part, a reduction on at least two variables in the set of variables (see, for example, Poulsen, column 10, lines 9-11 and 15-19, which shows that the routines in the library are called for each parallel region in the program, and Sundaresan, column 7, lines 13-16, which shows that the reduction operation performs a reduction on the values or variables).

With respect to claim 15, the limitations recited in the claim are analogous to the limitations recited in claim 1 (therefore, see Poulsen and Sundaresan as applied to claim 1 above). Poulsen in view of Sundaresan further discloses a machine-readable medium that provides instructions, that when executed by a set of one or more processors, enable the set of

processors to perform the recited operations (see, for example, Poulsen, column 8, lines 37-39, and column 6, lines 46-50).

With respect to claim 16, see Poulsen and Sundaresan as applied to claim 2 above.

With respect to claim 17, see Poulsen and Sundaresan as applied to claim 4 above.

With respect to claim 18, see Poulsen and Sundaresan as applied to claim 3 above.

With respect to claim 19, see Poulsen and Sundaresan as applied to claim 5 above.

With respect to claim 20, see Poulsen and Sundaresan as applied to claim 7 above.

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to Applicant's disclosure. U.S. Pat. No. 6,725,448 to Moriya et al. discloses a method and system for optimizing parallel processing.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael J. Yigdall whose telephone number is (571) 272-3707. The examiner can normally be reached on Monday through Friday from 7:30am to 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Q. Dam can be reached on (571) 272-3695. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MY

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